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Amendment and/or Response  
Reply to Office action of 4 December 2006

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**Amendments to the Claims:**

A clean version of the entire set of pending claims, including amendments to the claims, is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A circuit arrangement ~~(100)~~ for controlling at least one transistor ~~(10, 12, 14, ..., 18)~~, especially for controlling the resistance value of at least one MOS transistor with vanishing DC modulation, comprising: ~~characterized in that in addition to~~

at least one first reference element ~~(10, 20, 70)~~, which comprises at least one first reference transistor ~~(10)~~ with a first offset from the operating point, and

at least a second reference element ~~(12, 30, 40, 72, 74, 76)~~ is provided, which comprises at least a second reference transistor ~~(12)~~ with a second offset from the operating point equal in value but opposed in sign to the first offset,

wherein ~~in particular an arithmetic mean can be~~ taken of the first offset and the second offset for approximating and reaching an optimum operating point.

2. (Currently Amended) A circuit arrangement as claimed in claim 1, ~~characterized by including:~~

at least an external resistor ~~(78)~~ by means of which a reference current ~~(I<sub>ref</sub>)~~ produces a voltage ~~(U<sub>r</sub>)~~ on the basis of a reference voltage ~~(U<sub>ref</sub>)~~,

the first reference transistor ~~(10)~~, by means of which a first current ~~(I<sub>1</sub>)~~ corresponding in value and in sign to the reference current ~~(I<sub>ref</sub>)~~ produces a first voltage ~~(U<sub>1</sub>)~~,

at least a first buffer element ~~(20)~~ connected next in line to the drain connection ~~(10d)~~ of the first reference transistor ~~(10)~~ or to the source connection ~~(10s)~~ of the first reference transistor ~~(10)~~,

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at least a first resistor ~~(70)~~ connected next in line to the output connection ~~(20e)~~ of the first buffer element ~~(20)~~,

at least a second reference transistor ~~(12)~~ by means of which a second current ~~(12)~~ equal but opposed to the first current ~~(11)~~ produces a second voltage ~~(U2)~~,

at least a second buffer element ~~(30)~~ connected to the drain connection ~~(12d)~~ of the second reference transistor ~~(12)~~ or to the source connection ~~(12s)~~ of the second reference transistor ~~(12)~~,

at least an operational amplifier ~~(40)~~, in particular an inverting amplifier with amplification factor -1,

whose first, negative input connection ~~(40i1)~~ is connected next in line to the output connection ~~(30e)~~ of the second buffer element ~~(30)~~ and

whose second, positive input connection ~~(40i2)~~ is charged with the reference voltage ~~(Uref)~~, wherein the second voltage ~~(U2)~~ is capable of being inverted to an inverted second voltage ~~(U2inv)~~ with respect to the reference voltage ~~(Uref)~~,

at least a second resistor ~~(72)~~ connected next in line to the output connection ~~(40o)~~ of the operational amplifier ~~(40)~~,

at least a comparator element ~~(50)~~,

whose first, positive input connection ~~(50i1)~~ is connected next in line to the first resistor ~~(70)~~ and to the second resistor ~~(72)~~ in order to charge this first input connection ~~(50i1)~~ of the comparator element ~~(50)~~ with a mean voltage ~~(Um)~~ averaged over the first resistor ~~(70)~~ and the second resistor ~~(72)~~, and

whose second, negative input connection ~~(50i2)~~ is charged with the voltage ~~(Ur)~~ produced by means of the external resistor ~~(78)~~, and

at least a condenser element ~~(60)~~ connected next in line to the output connection ~~(50o)~~ of the comparator element ~~(50)~~, which can be charged and discharged by the comparator element ~~(50)~~ as a function of the result of a comparison between the mean voltage value ~~(Um)~~ and the voltage ~~(Ur)~~ produced by the external resistor ~~(78)~~, wherein the respective gates ~~(10g, 12g, 14g, ..., 18g)~~ of

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the first reference transistor ~~(10)~~, the second reference transistor ~~(12)~~ and of all further transistors to be controlled ~~(14, ..., 18)~~, as applicable, can be fed with the voltage  $(U_e)$  of condenser element ~~(60)~~ serving as a control voltage, ~~and/or~~ and wherein the optimum operating point corresponding to the control voltage  $(U_e)$  is reached, the moment the mean voltage value  $(U_m)$  corresponds to the voltage  $(U_r)$  produced by the external resistor ~~(78)~~.

3. (Currently Amended) A circuit arrangement as claimed in claim 2, ~~characterized in that~~ wherein the source connection ~~(10s)~~ of the first reference transistor ~~(10)~~ or the drain connection ~~(10d)~~ of the first reference transistor ~~(10)~~ and the source connection ~~(12s)~~ of the second reference transistor ~~(12)~~ or the drain connection ~~(12d)~~ of the second reference transistor ~~(12)~~ are chargeable with the reference voltage ~~(Uref)~~.

4. (Currently Amended) A circuit arrangement as claimed in claim 2, ~~characterized in that~~ wherein the first voltage  $(U_1)$  is lower than the reference voltage  $(U_{ref})$  ~~and/or~~ and the second voltage  $(U_2)$  is higher than the reference voltage  $(U_{ref})$ .

5. (Currently Amended) A circuit arrangement as claimed in claim 2, ~~characterized in that~~ wherein, at least a third resistor ~~(74)~~ is connected between the output connection ~~(30e)~~ of the second buffer element ~~(30)~~ and the first, negative input connection ~~(40i1)~~ of the operational amplifier ~~(40)~~, ~~and/or~~ and at least a fourth resistor ~~(76)~~ is connected parallel to the first, negative input connection ~~(40i1)~~ of the operational amplifier ~~(40)~~ and to the output connection ~~(40e)~~ of the operational amplifier ~~(40)~~.

6. (Currently Amended) A method of controlling ~~at least a transistor (10, 12, 14, ..., 18)~~, particularly of controlling the resistance value of at least one or more MOS transistor transistors with vanishing DC modulation, ~~characterized in that~~ wherein

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a first reference transistor ~~(10)~~ produces a positive voltage drop ~~(U1)~~,  
especially a positive DC voltage drop,

a second reference transistor ~~(12)~~ produces a negative voltage drop ~~(U2)~~,  
especially a negative DC voltage drop,

the negative voltage drop ~~(U2)~~ is inverted to an inverted voltage drop ~~(U2inv)~~

an arithmetic mean voltage value ~~(Um)~~ is formed from the positive voltage  
drop ~~(U1)~~ and the inverted voltage drop ~~(U2inv)~~ and is compared with an externally  
caused voltage drop ~~(Ur)~~, in particular an externally caused DC voltage drop, and

the resistance values of the first reference transistor ~~(10)~~, the second  
reference transistor ~~(12)~~ and any additional all further transistors ~~(14, ..., 18)~~  
whose resistance values are to be controlled, as applicable, are regulated by means  
of a control voltage ~~(Uc)~~ formed by the comparison of the mean voltage value ~~(Um)~~  
and the externally caused voltage drop ~~(Ur)~~.

7-10. (canceled)

11. (New) A device for controlling a resistance value of one or more MOS  
transistors, comprising:

a first reference element, including a first reference transistor adapted to  
produce a first voltage less than a reference voltage by a first offset voltage;

a second reference element, including,

a second reference transistor adapted to produce a second voltage  
greater than the reference voltage by the first offset voltage, and

a circuit adapted to convert the second voltage to a third voltage less  
than the reference voltage by the first offset voltage;

a resistor adapted to produce a fourth voltage from a voltage drop across the  
resistor as a result of a reference current passing therethrough;

a comparator adapted to compare the fourth voltage with an arithmetic mean  
of the first and third voltages; and

a condenser having a terminal connected to an output of the comparator,

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wherein the comparator is adapted to charge and discharge a control voltage at the terminal of the condenser in response to the comparison of the fourth voltage and the mean of the first and third voltages, and

wherein the control voltage is provided to a control terminal of each of the one or more MOS transistors whose resistance values are to be controlled, and to control terminals of the first and second reference transistors.

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